

Docket No. H1788

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant: Capodiec  
Serial No.: 10/677,154  
Filed: October 1, 2003  
For: **OPTICAL PROXIMITY CORRECTION (OPC) TECHNIQUE USING GENERALIZED FIGURE OF MERIT FOR PHOTOLITHOGRAPHIC PROCESSING**  
Art Unit: Not yet assigned  
Examiner: Not yet assigned

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
Washington, D.C. 20231

Sir:

1. Pursuant to 37 C.F.R. 1.97 and 1.98, and in compliance with 37 C.F.R. 1.56, the Office's attention is directed to the patents, pending applications, publications and other information listed on the attached PTO-1449. A copy of each listed document is enclosed except for: (a) pending applications, (b) those previously cited or submitted to the Office in the following application(s) upon which this application relies for an earlier filing date under 35 U.S.C. 120, or (c) U.S. patents and U.S. patent application publications if the filing date of the above-captioned patent application is after June 30, 2003:

Serial No.: \_\_\_\_\_  
Filing Date: \_\_\_\_\_

Regarding any document, publication or other information for which a date is not given on the attached PTO-1449, Applicant(s) believe(s) the same may qualify as "prior" art to this application and should be treated accordingly, although Applicant(s) reserve(s) the right to contest the prior art status of any document, publication or information, should issue arise.

2. Regarding each listed document that is not in the English language, an English-language translation accompanies this Statement as indicated on the attached PTO-1449 or a concise explanation of the relevance of the document is set forth in the following document(s):

- (a) \_\_\_ Copy of each English language version of a search report indicating the degree of relevance found by the foreign office of each document being submitted from the search report.
- (b) \_\_\_ Attachment entitled "Concise Explanation of Relevance of Non-English Language Documents".

3. Pursuant to 37 C.F.R. 1.97(b) this Statement is being filed (one must be checked):

- (a) X Within 3 months of the filing date or date of entry into the National Stage.
- (b) \_\_\_ Before the mailing date of a first Office Action on the merits. If this Statement is not filed before the mailing date of a first Office Action on the merits, the required certification is given below or, in the absence thereof, the Office is authorized to charge the required fee set forth in 37 C.F.R. 1.17(p) to Deposit Account No. 18-0988 for consideration of this Statement.
- (c) \_\_\_ Before the mailing date of a first Office Action on the merits after a first or second submission under 37 C.F.R. 1.129(a).
- (d) \_\_\_ After the period set forth in 37 C.F.R. 1.97(b) but before the mailing date of either a final action or a notice of allowance.

- (1) \_\_\_ The required certification is given below, or
- (2) \_\_\_ Enclosed is a check covering the fee set forth in 37 C.F.R. 1.17(p) for consideration of this Statement, or
- (3) \_\_\_ Charge the fee set forth in 37 C.F.R. 1.17(p) to Deposit Account No. 18-0988.
- (e) \_\_\_ After the mailing date of either a final action or a notice of allowance, but before payment of the issue fee. Petition hereby is made for consideration of this Statement and the required certification is indicated below.
- (1) \_\_\_ Enclosed is a check covering the fee set forth in 37 C.F.R. 1.17(p), or
- (2) \_\_\_ Charge the fee set forth in 37 C.F.R. 1.17(p) to Deposit Account No. 18-0988.
4. Certification (if applicable)
- (a) \_\_\_ The undersigned hereby certifies that each item of information contained in this Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than 3 months prior to the filing of this Statement.
- (b) \_\_\_ The undersigned hereby certifies that no item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the undersigned's knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. 1.56(c) more than 3 months prior to the filing of this Statement.
5. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 18-0988.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

By   
M. David Galin, Reg. No. 41,767

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**CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8**

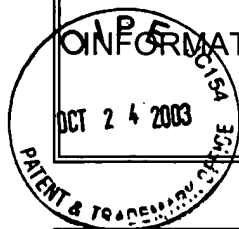
I hereby certify that this paper and the documents enclosed herewith are being deposited on the date indicated below with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Date: October 22, 2003

  
M. David Galin

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Form PTO-1449 (Modified)	Atty Docket No. H1788	Serial No. 10/677,154
<b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b> (Use several sheets if necessary)	Applicant: Capodieci	
	Filing Date 10/1/03	Group Not yet assigned



## U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Sub-class	Filing Date if Appropriate
	6,243,855	6/2001	Kobayashi, et al.			
	6,381,731	4/2002	Grodd			
	6,397,372	5/2002	Bozkus, et al.			
	6,415,421	7/2002	Anderson, et al.			
	6,425,113	7/2002	Anderson, et al.			
	6,430,737	8/2002	Cobb, et al.			

## OTHER ART

Examiner Initial	Author, Title, Date, Pertinent Pages, etc.
	Schellenberg, et al. A New Process Monitor for Reticles and Wafers: The MEEF Meter, Presented at SPIE's Microlithography 2000 Symposium, February 27 to March 3, 2000.
	Schulze and Lacour. A GDS-based Mask Data Preparation Flow - Data Volume Containment by Hierarchical Data Processing. Mentor Graphics; Deep Submicron Technical Publications, November 2002.
	Torres and Maurer. Alternatives to Alternating Phase Shift Masks for 65nm. Mentor Graphics; Deep Submicron Technical Publications, November 2002.
	Torres, et al. Design Verification Flow for Model Assisted Double Dipole Decomposition. Mentor Graphics; Deep Submicron Technical Publications, September 2002.
	Capodieci, et al. Effects of Advanced Illumination Schemes on Design Manufacturability and Interactions with Optical Proximity Corrections. Mentor Graphics; Deep Submicron Technical Publications, September 2000.
	Cobb and Sahouria. Hierarchical GDSII-based fracturing and job deck system. Mentor Graphics; Deep Submicron Technical Publications, November 2001.

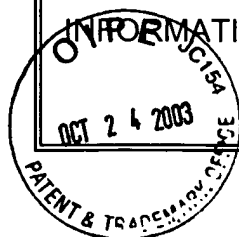
EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**Information Disclosure Statement PTO-1449 (Modified)**

The identification of any reference is not intended to be, and should not be understood as being, an admission that such publication, in fact, constitutes "prior art" within the meaning of applicable law since, for example, a given reference may have a later effective date than first seems apparent or the reference may have an effective date which can be antedated. The "prior art" status of any reference is a matter to be resolved during prosecution.

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## OTHER ART

Examiner Initial	Author, Title, Date, Pertinent Pages, etc.
	Schellenberg. Impact of RET on Physical Layouts. Mentor Graphics; Deep Submicron Technical Publications, April 2001.
	Schellenberg, et al. OPC Beyond 0.18 $\mu\text{m}$ : OPC on PSM Gates. Mentor Graphics. Mentor Graphics; Deep Submicron Technical Publications, November 2001. Presented at SPIE's Microlithography 2000 Symposium February 27 - March 3, 2000.
	Torres, et al. RET Compliant Cell Generation for sub-130nm Processes. Mentor Graphics; Deep Submicron Technical Publications, June 2002.
	Vandenberghe, et al. (Sub-) 100nm Gate Patterning Using 248nm Alternating PSM. Mentor Graphics; Deep Submicron Technical Publications, May 2001.
	Granik, et al. Sub-resolution Process Windows and Yield Estimation Technique Based on Detailed Full-chip CD Simulation. Mentor Graphics; Deep Submicron Technical Publications, September, 2000.
	Schellenberg and Moore. Verifiable OPC Methodologies. Mentor Graphics; Deep Submicron Technical Publications, March, 1999.

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